Attorney Docket No. YOR920030306US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): M. Kapur et al.
Docket No.: YOR920030306US1
Serial No.: 10/650,222
Filing Date: August 28, 2003
Group: 2138
Examiner: Saqib Javaid Siddiqui

Title: Self-Synchronizing Pseudorandom Bit Sequence Checker

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
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Sir:

The remarks below are submitted in response to the Notification of Non-Compliant Appeal Brief dated July 25, 2007 (hereinafter "Notification"), in the above-identified application. The Appeal Brief at issue was filed June 29, 2007.

For the reasons identified herein, Applicants (hereinafter "Appellants") believe that the Notification is improper and should be withdrawn, and that the June 29, 2007 Appeal Brief is in fact compliant with all relevant statutes and regulations.

Notwithstanding the traversal, a revised Summary section is submitted herewith to conform to the subjective preference indicated in the Notification.

REMARKS

In the Notification of Non-Compliant Appeal Brief dated July 25, 2007, the June 29, 2007 Appeal Brief is objected to as failing to contain a concise explanation of the independent claims involved in the appeal. More specifically, at page 1, last paragraph of the Notification, the Patent Appeal Center Specialist alleges that the "summary of claimed subject matter fails to identify and map each independent claim (12) to the specification by page and line number and to the drawings, if any. The appellant may wish to only submit the defective section of the brief."

The relevant regulation governing the summary of claimed subject matter in an Appeal Brief is 37 C.F.R. §41.37(c)(1)(v), which provides as follows with emphasis supplied:

> (v) *Summary of claimed subject matter.* A concise explanation of the subject matter defined in each of the independent claims involved in the appeal, which shall refer to the specification by page and line number, and to the drawing, if any, by reference characters. For each independent claim involved in the appeal and for each dependent claim argued separately under the provisions of paragraph (c)(1)(vii) of this section, every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters.

Appellants respectfully contend that the 37 C.F.R. §41.37(c)(1)(v) merely requires a "concise explanation of the subject matter defined in each of the independent claims involved in the appeal, which shall refer to the specification by page and line number, and to the drawing, if any, by reference characters." Indeed, MPEP §1201.05 states that "[w]hile reference to page and line number of the specification requires somewhat more detail than simply summarizing the invention, it is considered important to enable the Board to more quickly determine where the claimed subject matter is described in the application."

Appellants respectfully submit that the summary provided in the June 29, 2007 Appeal Brief contained a "concise explanation of the subject matter defined in each of the independent claims involved in the appeal" which referred to the "specification by page and line number" and to the

drawings by reference characters in "more detail than simply summarizing the invention" in a manner more than sufficient to enable the Board to quickly "determine where the claimed subject matter is described in the application."

Accordingly, Appellants submit that the summary provided in the June 29, 2007 Appeal Brief is proper and fully compliant with 37 C.F.R. §41.37(c)(1)(v). The Notification of Non-Compliant Appeal Brief is therefore believed to have been issued in error, and should be withdrawn.

Notwithstanding the traversal, Appellants submit herewith a revised Summary section, solely to conform to the subjective preference of the Examiner.

Respectfully submitted,

Date: August 27, 2007

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SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the method comprising the steps of: delaying the PRBS received by the device to generate a delayed PRBS; detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and prohibiting propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

An illustrative embodiment of the recited method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device (e.g., PRBS checker 430 in FIG. 4), the method comprising the steps of: delaying the PRBS received by the device (e.g., shift registers R0, R1 and R2 in FIG. 4) to generate a delayed PRBS (e.g., Specification, page 6, lines 24-25, "The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0"); detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device (e.g., Specification, page 6, lines 25-26, "The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1"); and prohibiting propagation of the detected error bit in the delayed PRBS (e.g., Specification, page 7, lines 1-3, "An error in the DUT output stream is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2."); wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device (e.g., RX1 in FIG. 4, Specification, page 6, lines 25-26, "The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1").

Independent claim 6 recites an apparatus for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the apparatus comprising: a memory; and at least one processor coupled to the memory and operative to: (i) delay the PRBS received by the device to generate a delayed PRBS; (ii) detect the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by

the device; and (iii) prohibit propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

An illustrative embodiment of the recited apparatus (e.g., that described with reference to FIG. 12 in the Specification at page 9, lines 8-10) for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device (e.g., PRBS checker 430 in FIG. 4), the apparatus comprising: a memory (e.g., Specification, page 9, lines 8-10, "the PRBS checkers (and generators) described above may be implemented in accordance with...a memory"); and at least one processor (e.g., Specification, page 9, lines 8-10, "the PRBS checkers (and generators) described above may be implemented in accordance with a processor for controlling and performing the various operations described herein") coupled to the memory and operative to: (i) delay the PRBS received by the device (e.g., shift registers R0, R1 and R2 in FIG. 4) to generate a delayed PRBS (e.g., Specification, page 6, lines 24-25, "The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0"); (ii) detect the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device (e.g., Specification, page 6, lines 25-26, "The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1"); and (iii) prohibit propagation of the detected error bit in the delayed PRBS (e.g., Specification, page 7, lines 1-3, "An error in the DUT output stream is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2."); wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device (e.g., RX1 in FIG. 4, Specification, page 6, lines 25-26, "The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1").

Independent claim 11 recites an article of manufacture for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, comprising a machine readable medium containing one or more programs which when executed implement the steps of: delaying the PRBS received by the device to generate a delayed PRBS; detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a

portion of the PRBS received by the device; and prohibiting propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

An illustrative embodiment of the recited article of manufacture (e.g., Specification, page 9, lines 21-24) for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device (e.g., PRBS checker 430 in FIG. 4), comprising a machine readable medium (e.g., Specification, page 9, lines 21-23, "computer software including instructions or code for performing the methodologies of the invention, as described herein, may be stored in one or more of the associated memory devices (e.g., ROM, fixed or removable memory)") containing one or more programs which when executed (e.g., Specification, page 9, lines 21-25, "computer software...when ready to be utilized, loaded in part or in whole (e.g., into RAM) and executed by a CPU") implement the steps of: delaying the PRBS received by the device (e.g., shift registers R0, R1 and R2 in FIG. 4) to generate a delayed PRBS (e.g., Specification, page 6, lines 24-25, "The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0"); detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device (e.g., Specification, page 6, lines 25-26, "The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1"); and prohibiting propagation of the detected error bit in the delayed PRBS (e.g., Specification, page 7, lines 1-3, "An error in the DUT output stream is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2."); wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device (e.g., RX1 in FIG. 4, Specification, page 6, lines 25-26, "The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1").

Independent claim 12 recites an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the apparatus comprising: a shift register chain; a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output

PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

An illustrative embodiment of the recited apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device (e.g., DUT 420 in FIG. 4) in response to an input PRBS received by the device, the apparatus comprising: a shift register chain (e.g., shift registers R0, R1 and R2 in FIG. 4); a logic gate (e.g., RX1 in FIG. 4) coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS (e.g., Specification, page 6, lines 25-26, "The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1"); and at least one logic detector (e.g., one detector 437 in FIG. 4) coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain (e.g., Specification, page 7, lines 1-3, "An error in the DUT output stream is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2.").